A Microprocessor-Based PSK Modem for Packet Transmission Over Satellite Channels

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Abstract—This paper describes a microprocessor-based modem developed for use in a packet switching network over satellite channels. This digital modem can process both BPSK and QPSK packets with near optimum error rate performance over channels with marginal signal energy-to-noise density ratio.

Of principal concern is the development of the discrete time algorithms which form the basis of the microinstruction program. The processing of a packet can be decomposed into two basic stages: (1) the detection of the packet preamble and the rapid estimation of signal parameters (symbol timing and carrier frequency offset) for the specific packet, and (2) the demodulation of the data portion of the packet including the tracking of both symbol timing and carrier offset phase, phase ambiguity resolution and data symbol estimation.

The paper concludes with details on the performance of the modem under operational conditions and a brief discussion of implementation of the processor.

1.0 INTRODUCTION

THIS paper describes various detection, estimation and demodulation algorithms that have been developed and implemented in a microprocessor-based satellite communication modem. This modem was designed for use in a packet switching network, using binary or quaternary phase-shift-keyed (BPSK or QPSK) modulation. The requirements of a packet-switched network pose several challenges to the modem designer. Packets arrive at the receiver at random intervals from various transmitters in the network. The demodulator must quickly detect the presence of each packet and recover the data contained within it. Operation with limited channel bandwidth and a marginal signal-to-noise ratio requires the implementation of near-optimum detection, estimation and demodulation functions.

Communications users in a packet-switched network transmit blocks of data (packets) over a common channel. Packet lengths are typically on the order of 10^3 data bits (the length of a given packet may even be a random variable within a fixed range). The packet protocols and scheduling algorithms, also major elements in the system design, are beyond the scope of this paper and generally do not impact modem design; however, other characteristics of packet-switched networks do influence the modem. The throughput of a packet-switched network is affected by factors such as the probability of packet contention (two or more users attempting to send a packet at the same time), and system overhead (such as the lengths of packet preambles and scheduling information), as well as the need for retransmission due to the possibility of receiving a packet corrupted by one or more errors due to noise on the channel.

In the packet-switched network, for which this modem was designed, it is desirable to minimize the length of the preamble while retaining the ability of the modem to detect and demodulate packets. Because error control coding is used, the received symbol energy-to-noise density (E_s/N_0) can be as low as 1 dB. This factor leads to the choice of a 96-symbol, BPSK preamble composed of alternating zeros and ones. This preamble has the favorable properties of allowing an easy detection algorithm, plus a maximum number of symbol transitions upon which an estimate of symbol phase (timing) can be made. The lowest E_s/N_0 case uses BPSK modulation in conjunction with a rate 1/2*, constraint length 7, convolutional code and a Viterbi decoder. This combination results in a bit error probability of less than 10^{-4}, assuming near optimum demodulation. In addition, a parity tail or "checksum" inserted on the end of each packet (before convolutional encoding) is used to detect errors which are not corrected by the decoder. The preamble length, modulation and coding parameters were chosen based on the goal of maximizing network efficiency (throughput).

The satellite channel for this application is a relatively narrowband channel in a frequency division-multiple access (FDMA) system. The modem is designed for BPSK and QPSK modulation with a 32 kHz *symbol* rate (a symbol is one transmitted bit in BPSK, and 2 bits in QPSK). Serious constraints on out-of-band power require that a filter with a sharp rolloff in the stop band be used at the transmitter. Similarly, the receiver must use a selective filter to minimize the effects of adjacent and cochannel interference. As an additional constraint, the transmit and receive filtering should not result in a significant degradation in error rate performance as a function of energy-to-noise, compared to ideal matched filter detection of infinite bandwidth PSK in white Gaussian noise.

Before developing the details of packet demodulation, it is useful to describe qualitatively the nature of packet transmission and demodulation. A packet is formed by the transmission of a 96-symbol BPSK (1 bit/symbol) preamble of alternating zeros and ones, followed by a number of BPSK (1 bit/symbol) or QPSK (2 bits/symbol) data symbols. These symbols include a fixed start of message sequence which is used for frame synchronization and phase ambiguity resolution. The packet is bandlimited at the transmitter and then modulated by quadrature carriers. The channel introduces

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* Thus, in this case, the bit energy to noise density (E_b/N_0) is 4 dB.

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additive white Gaussian noise (AWGN) to the signal which is then presented to the receiver. The analog portion of the receiver first mixes the incoming signal by quadrature sinusoids which are at a frequency within 2 kHz of the carrier (±2 kHz is the received carrier uncertainty). This carrier frequency offset and its phase must be estimated by the processor so that the unwanted modulation which results can be removed numerically. Before the in-phase and quadrature signals are sampled and sent to the processor, both are passed through low pass filters with a noise bandwidth of approximately 18 kHz. This wider filter (as opposed to the Nyquist filter with noise bandwidth of 16 kHz) was chosen so that, when the frequency offset was maximum (±2 kHz), the signal would not be seriously attenuated. The two filtered signals are then sampled at 64 kHz (twice the symbol rate) and presented to the microprocessor for numerical processing.

The numerical processing of a packet can be decomposed into two stages. The first, the preamble stage, involves the detection of the presence of a packet. Since the arrival of a packet is a random event, an estimate of the symbol phase (timing) must be made during this stage as well as estimates of the carrier frequency offset and phase. Once this has been completed, the processor (which has complete control of the sampling clock) adjusts the sampling instants based on the timing estimate, and proceeds to the second stage of processing.

The second stage, the data recovery stage, involves the tracking of both symbol timing and frequency offset and phase so that estimates of the data symbols can be made. For symbol time tracking, an error signal is derived from the incoming samples, which is used to drive a numerical first-order phase-locked loop. The output of the PLL is used to adjust the sampling clock. The carrier frequency offset and phase tracking involves the computation of an error signal which is used to drive a second-order phase-locked loop. (The error signal calculation for QPSK symbols differs slightly from the error signal used for BPSK.) The output from this second numerical PLL is used to numerically rotate the samples as they enter the processor. In addition to these two tracking functions, the rotated data are filtered by a simple finite impulse response (FIR) digital filter which helps to reduce the effects of intersymbol interference by giving the received data a spectral shape which is closer to satisfying the Nyquist criterion. A flowchart of the entire computational process is shown in Figure 1.1.

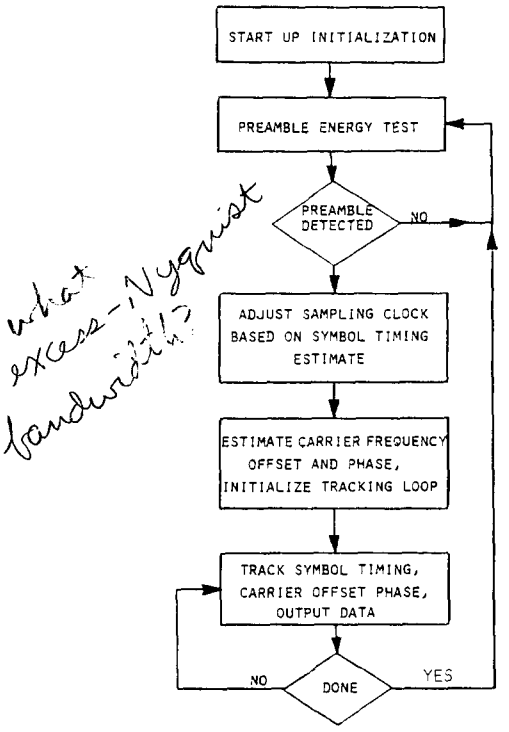

Figure 1.1. General Algorithm.

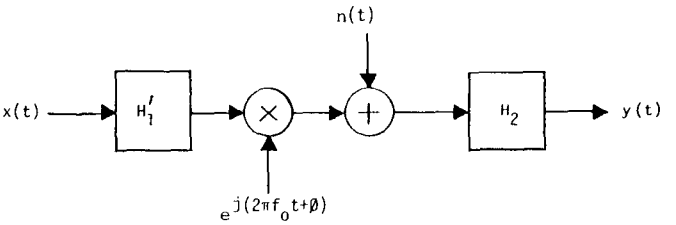

Figure 2.1. The QPSK/BPSK Model (Complex Signals).

2.0 MODELS

In this section we begin the development of the set of discrete time algorithms which are used for the demodulation of packets at the receiver. The discrete time signals (sequences) are obtained by sampling an analog (continuous) signal. We begin with the model of Figure 2.1 which incorporates the use of complex signals. A derivation of this model from the real signal model is given in Appendix A. The complex signal

$$x(t) = \sum_i (a_i - jb_i)p(t - iT) = x_1(t) + jx_2(t) \qquad (2.1)$$

where

$$p(t) = \begin{cases} 1; & -T/2 \leq t < T/2 \\ 0; & \text{otherwise} \end{cases} \qquad (j \equiv \sqrt{-1})$$

is the data sequence $\{(a_i - jb_i)\}$ modulated by rectangular pulses. The transmitter filters this signal by a real filter $H_1'(f)$. The carrier frequency offset is introduced by the modulation of the transmitted signal by the complex sinusoid $e^{j(2\pi f_0 t+\phi)}$. The channel introduces additive white Gaussian noise which is represented by the complex signal $\eta(t)$. The receiver filters this composite signal by the real filter $H_2(f)$ which is then presented to the processor for sampling and numerical processing.

The microprocessor samples the incoming complex signal $y(t)$ at twice the data rate. This results in two complex sequences (even and odd),

$$y_e(n) = y(t)|_{t=\tau+nT}$$

$$= \sum_i (a_i - jb_i)f(\tau + nT - iT)e^{j[2\pi f_0(\tau+nT)+\phi]} + \tilde{\eta}(\tau + nT) \qquad (2.2a)$$

$$y_0(n) = y(t)|_{t=\tau+nT+T/2}$$
$$= \sum_i (a_i - jb_i) f(\tau + nT - iT + T/2) \cdot e^{j[2\pi f_0(\tau+nT+T/2)+\phi]} + \tilde{\eta}(\tau + nT + T/2) \quad (2.2b)$$

where $f(t)$ is the response of the cascade of $H_1'(f)$ and $H_2(f)$ to the rectangular pulse $p(t)$ and $\tilde{\eta}(t)$ is the filtered version of $\eta(t)$ (cf. (A.3) of Appendix A).

These two sequences are used by the processor for packet demodulation. The demodulation of a packet can be decomposed into two distinct stages. The first stage involves the detection of a packet preamble, and the estimation of certain parameters (namely the symbol phase and the offset frequency and phase) which are essential to the demodulation of the data portion of the packet. Since both BPSK and QPSK packets have the same 96-bit preamble, this stage of the processing is identical for all packets. Define

$$a_i = b_i = \frac{1}{\sqrt{2}}(-1)^i, \qquad 0 \leqslant i < 96$$

as the packet preamble. Then the received preamble sequences are $0 \leqslant n < 96$

$$y_e(n) = \sum_i (-1)^i f(\tau + (n-i) \cdot T) e^{j[2\pi f_0(\tau+nT)+\phi-\pi/4]} + \tilde{\eta}_e(n) \quad (2.3a)$$

$$y_0(n) = \sum_i (-1)^i f(\tau + (n-i) \cdot T + T/2) \cdot e^{j[2\pi f_0(\tau+nT+T/2)+\phi-\pi/4]} + \tilde{\eta}_0(n). \quad (2.3b)$$

Due to the severe filtering on the rectangular pulses, the received waveform of the preamble can be approximated by a sinusoid of period $2T$, i.e., $0 \leqslant n < 96$

$$y_e(n) \approx \cos\left(\frac{\pi\tau}{T} + n\pi\right) e^{j2\pi f_0 nT+\phi'} + \tilde{\eta}_e(n) \quad (2.4a)$$

$$y_0(n) \approx \sin\left(\frac{\pi\tau}{T} + n\pi\right) e^{j2\pi f_0 nT+\phi''} + \tilde{\eta}_0(n) \quad (2.4b)$$

during the preamble. Since $f_0 T$ is small, we can also make the approximation $\phi - \pi/4 = \phi' = \phi''$. These preamble sequences, embedded in the channel noise, are detected by the processor and then estimates of τ, f_0 and ϕ are obtained.

The second stage of packet demodulation involves tracking both the symbol timing and carrier frequency offset and phase. These tracking functions are initialized based on the estimates obtained in the first stage. The derivation of the error signals for carrier frequency offset tracking are dependent upon the modulation of the data portion (BPSK or QPSK) of the packet. Both cases will be considered here. The sequences during the data portion are

$$y_e(n) = \sum_i (a_i - jb_i) f(\tau_E(n) + (n-i) \cdot T) e^{j\phi_E(n)} + \tilde{\eta}_e(n) \quad (2.5a)$$

$$y_0(n) = \sum_i (a_i - jb_i) f(\tau_E(n) + (n-i) \cdot T + T/2) e^{j\phi_E(n)} + \tilde{\eta}_0(n) \quad (2.5b)$$

where the sequences τ_E, ϕ_E are the tracking errors in timing and carrier offset phase. Assuming these errors are small, the processor outputs the even sequence as data, since

$$y_e(n) \approx \sum_i (a_i - jb_i) f((n-i) \cdot T) + \tilde{\eta}_e(n) \quad (2.6)$$

where $f((n-i) \cdot T)$ are the intersymbol interference (ISI) coefficients. In the absence of intersymbol interference $f((n-i) \cdot T) = \delta(n-i)$, the Kronecker delta function, in which case,

$$y_e(n) \approx a_n - jb_n + \tilde{\eta}_e(n). \quad (2.7)$$

3.0 ACQUISITION AND DEMODULATION ALGORITHMS

During the first stage of packet processing, the preamble stage, the processor must detect the presence of a randomly arriving packet embedded in channel noise. This detection is complicated by the fact that an unknown frequency offset modulates the preamble. We have noted that the even (odd) sequence is proportional to the cosine (sine) of the unknown symbol phase during the preamble portion. Intuitively, if we form the two "matched" filters (Figure 3.1)

$$\beta_0(n) = \sum_{k=n}^{n+N-1} (-1)^k y_e(k) = \sum_{k=n}^{n+N-1} \cos\left(\frac{\pi\tau}{T}\right) e^{j[2\pi f_0 Tk+\phi']} + (-1)^k \tilde{\eta}_e(k) \quad (3.1a)$$

$$\beta_1(n) = \sum_{k=n}^{n+N-1} (-1)^k y_0(k) = \sum_{k=n}^{n+N-1} \sin\left(\frac{\pi\tau}{T}\right) e^{j[2\pi f_0 Tk+\phi'']} + (-1)^k \tilde{\eta}_0(k) \quad (3.1b)$$

we would expect the magnitude squared of these filter outputs,

$$\gamma_0(n) = |\beta_0(n)|^2; \qquad \gamma_1(n) = |\beta_1(n)|^2 \quad (3.2)$$

to remain approximately constant (proportional to the noise variance, σ^2) before the arrival of a preamble, and to begin to grow linearly as the preamble is presented to the processor. If we assume for the moment that $f_0 = 0$, then we could set a

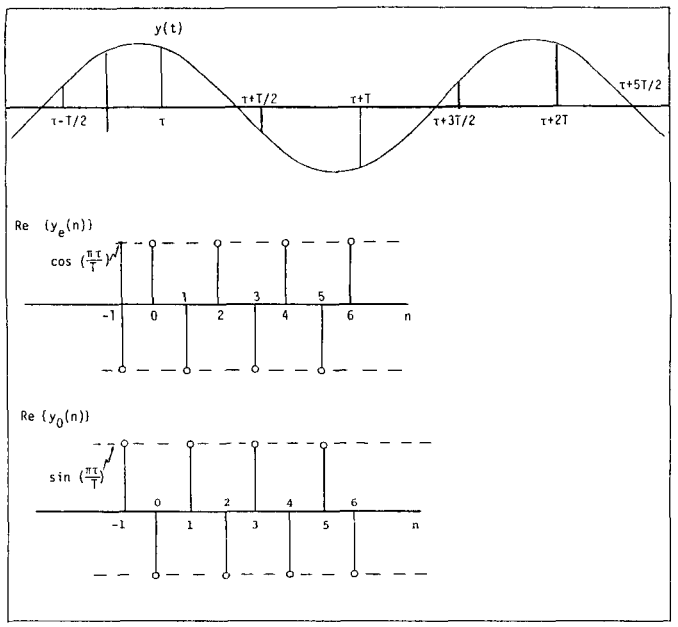

Figure 3.1. Samples of Preamble in Noiseless Environment and $f_0 = \phi = 0$.

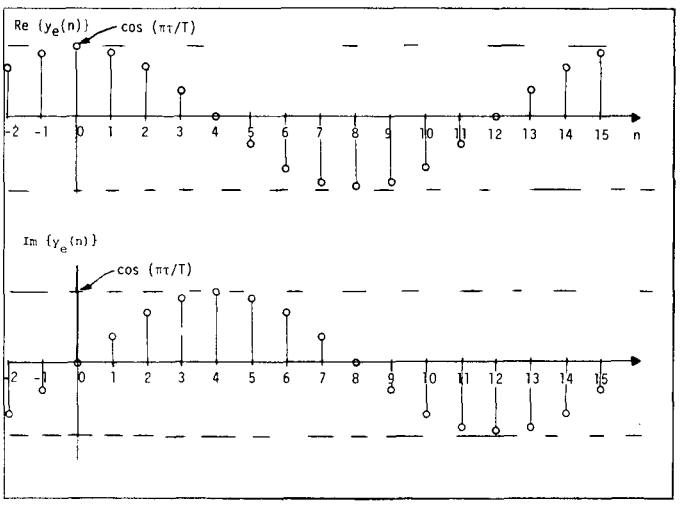

Figure 3.2. Samples of Preamble in Noiseless Environment and $f_0T = 1/16$, $\phi = 0$.

threshold to be used to declare the presence of a packet when max $\{\gamma_0, \gamma_1\}$ crossed the threshold. We could then estimate τ based on the relative sizes of γ_0 and γ_1. Two problems exist with this scheme. First, f_0 is, in general, not zero, but is constrained to be in the range,

$$|f_0T| \leqslant 1/16. \tag{3.3}$$

In the worst case ($|f_0T| = fT_{\max} = 1/16$), the filter outputs due to the signal would be zero if N (the length of summation) were 16 (see Figure 3.2). Thus, we must choose N to be relatively small (say, $N = 4$) so that we do not lose excessive signal energy due to the offset. Since it is desirable to have a longer summation (integration) period, a postdetection summation must be performed, i.e.,

$$\beta_0(n) = \sum_{k=n}^{n+3} (-1)^k y_e(k); \qquad \beta_1(n) = \sum_{k=n}^{n+3} (-1)^k y_0(k) \tag{3.4}$$

$$\gamma_0(n) = \sum_{k=n}^{n+15} |\beta_0(4k)|^2; \qquad \gamma_1(n) = \sum_{k=n}^{n+15} |\beta_1(4k)|^2. \tag{3.5}$$

Since the postdetection summation interval was chosen as 16, the overall summation interval is 64. Since the preamble is 96 bits long, this scheme allows the processor a window of 32 bits in which to detect a preamble (it is desired not to detect too early for reasons that will become apparent). Note that we could still estimate the timing phase; but this leads us to the other problem with the previously described strategy; namely, the difficulty of determining an estimate of the phase from the values of γ_0 and γ_1. To obtain this estimate, the following approach was used. We can form the set of sequences,

$$y_e'(n) = \frac{1}{\sqrt{2}}(y_e(n) + y_0(n));$$

$$y_0'(n) = \frac{1}{\sqrt{2}}(y_e(n) - y_0(n)) \tag{3.6}$$

$$\beta_2(n) = \sum_{k=n}^{n+3} (-1)^k y_e'(k); \qquad \beta_3(n) = \sum_{k=n}^{n+3} (-1)^k y_0'(k) \tag{3.7}$$

$$\gamma_2(n) = \sum_{k=n}^{n+15} |\beta_2(4k)|^2; \qquad \gamma_3(n) = \sum_{k=n}^{n+15} |\beta_3(4k)|^2 \tag{3.8}$$

which have maxima for values of τ which are between the points where γ_0 and γ_1 are maximum. Figure 3.3 shows a plot of the gammas vs. τ when the preamble is present without noise. It is easy to see that the maxima of these four sequences are equally spaced on the interval $0 \leqslant \tau < T$. Thus, the modified algorithm involves the computation of the four values of gammas, taking the maximum, say, γ_i, and determining whether its value exceeded a predetermined threshold. If the threshold was satisfied, a timing phase estimate is based solely on which gamma, i.e., γ_i, was maximum. In the absence of noise, this would lead to an error in the estimate, τ_E, in the range $-T/8 \leqslant \tau_E \leqslant T/8$.

In the presence of noise, this scheme leads to a slight bias toward γ_2 and away from γ_3. The reason for this is the fact that the cross correlation between the sequences $\tilde{\eta}_e$ and $\tilde{\eta}_0$ is not zero. This tends to increase the noise variance of the β_2's (since a sum of $\tilde{\eta}_e$ and $\tilde{\eta}_0$ is computed) while the noise vari-

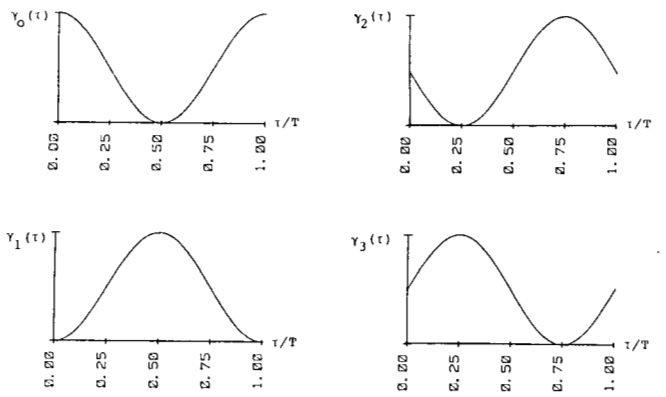

Figure 3.3. γ_i Functions vs. τ During Preamble (Without Noise).

ance of the β_3's is slightly reduced (a difference between $\tilde{\eta}_e$ and $\tilde{\eta}_0$ is taken). Simulations, to be described in Section 4.0, have shown that this effect introduces little degradation in performance of the detection and symbol timing phase estimation algorithm. In fact, this scheme has proven to be quite robust in the presence of noise.

The final step of the first stage is the estimation of the carrier offset frequency and phase f_0, ϕ of the packet. We begin by obtaining an approximation for the set of 16 β_i's which are used in the computation of γ_i. Let us define for $N = 4$, the reduced set of filter outputs $\hat{\beta}_0(n)$ as

$$\hat{\beta}_0(n) \equiv \beta_0(4n) = \cos\left(\frac{\pi\tau}{T}\right) \sum_{k=4n}^{4n+3} e^{j[2\pi f_0 Tk+\phi]} + \hat{\eta}_0(n) \tag{3.9}$$

and since $|f_0 T| \ll 1$

$$\hat{\beta}_0(n) \approx c_0(\tau) e^{j[8\pi f_0 Tn+\phi]} + \hat{\eta}_0(n) \tag{3.10}$$

where $\tilde{\eta}_0(n) = \Sigma_{k=4n}^{4n+3} (-1)^k \tilde{\eta}_0(k)$. Similarly, for each i, we can approximate

$$\hat{\beta}_i(n) \approx c_i(\tau) e^{j[8\pi f_0 Tn+\phi]} + \hat{\eta}_i(n); \qquad i = 0, 1, 2, 3 \tag{3.11}$$

where the functions $c_i(\tau)$ are real and fixed for a given τ. We use the set of 16 β_i's which compose the maximum γ_i, which are most likely to yield the sequence with the largest constant c_i. We can now obtain an estimate of f_0 by forming a series of discrete bandpass filters centered at various points in the range of $-4fT_{\max} \leqslant f_c T \leqslant 4fT_{\max}$. The filter with the maximum energy at the output leads to the estimate of f_0. Note, if the processor detects the preamble early, some of the early β_i's will be composed of noise which will only tend to degrade our estimate of f_0. In the actual modem, 16 discrete filters are computed using the discrete Fourier transform formula,

$$H_{f_c} = \sum_{k=M-15}^{M} \beta_i(k) e^{-j2\pi f_c k} \tag{3.12}$$

where M is such that $\max\{\gamma_0, \gamma_1, \gamma_2, \gamma_3\} = \gamma_i(M) >$ Threshold.

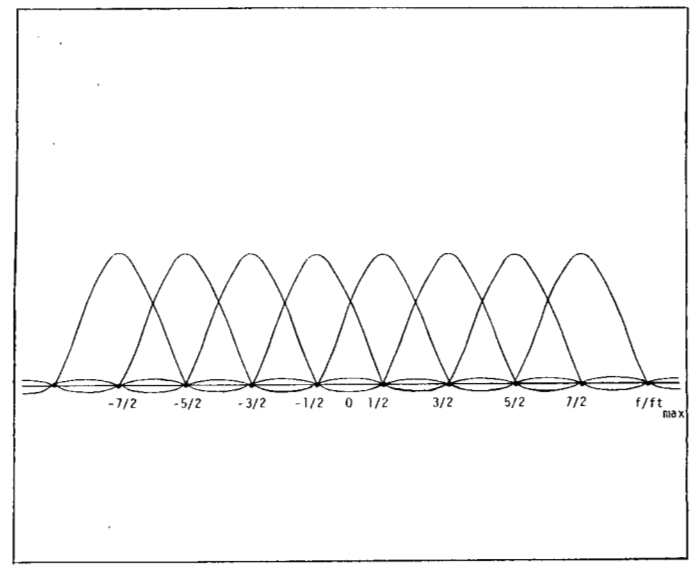

Figure 3.4. The 8 Orthogonal Filters for Initial Estimate of f_0.

First, eight orthogonal filters are formed in the range $-4fT_{\max} < f_c T < 4fT_{\max}$ (the factor of four appears due to the fact that $\hat{\beta}_i(n)$ is computed once for every four preamble symbols). The eight chosen filters are plotted in Figure 3.4. The center frequencies of these filters are $\pm 1/2fT_{\max}$, $\pm 3/2fT_{\max}$, $\pm 5/2fT_{\max}$, $\pm 7/2fT_{\max}$. Once the filter with the largest magnitude squared is found, say $\max_{f_c}\{H_{f_c}\} = H(f')$, a sequential search is made using eight more filters in the interval near f'. This search is best described through an example. Suppose f' were the location of the orthogonal filter with the most energy. Two filters, one at $f' - 1/2fT_{\max}$ and one at $f' + 1/2fT_{\max}$ would be computed. The largest of the three filters ($f' - 1/2fT_{\max}$, f', $f' + 1/2fT_{\max}$) would be chosen, say, $f' + 1/2fT_{\max}$. Next, two more filters, $f' + 1/4fT_{\max}$ and $f' + 3/4fT_{\max}$, would be computed and the maximum of the three would be chosen. This process continues for a total of four steps (8 filters).

An example of a sequential search is given in Figure 3.5. The heights of the impulses represent the relative size of the filter outputs. In this example, f' was chosen as zero and the numbers next to the impulses (which represent the filter outputs) indicate order of calculation, leading to a choice of the filter at $7/16fT_{\max}$. In the absence of noise, this search method would lead to an error in the estimate f_E, of $|f_E| \leqslant 1/64fT_{\max}$. With $T = 1/32$ ms and $fT_{\max} = 1/16$, this results in an error of less than 32 Hz.

Once an estimate of f_0 is made, the phase of the filter with the maximum output is used as the estimate of ϕ. For example, if $f_c = 4f_0$, then

$$H_{f_c} = \sum_{k=M-15}^{M} \hat{\beta}_i(n) e^{-j8\pi f_0 n} = 16 c_i(\tau) e^{j\phi} + \hat{\eta} \tag{3.13}$$

which would have a phase equal to ϕ (ignoring the noise term). Once this computation is complete, the processor is ready to begin stage two of the packet demodulation.

The second stage of packet demodulation involves the tracking of both symbol timing and carrier phase, and esti-

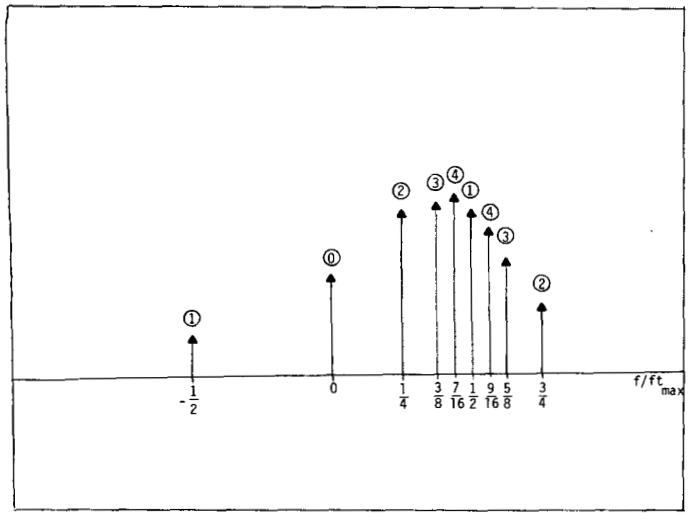

Figure 3.5. Example of Sequential Search.

mating the values of the data symbols (see Figure 3.6). The initialization of these tracking functions is based upon the estimates obtained from the preamble stage. We will return to this initialization procedure after considering the algorithms which implement these functions. The data demodulation stage of processing begins by sampling $y(t)$ at times $\tau_E(n)$ and $\tau_E(n) + T/2$ which results in the two samples $y_e(n)$ and $y_0(n)$

$$y_e(n) = \sum_i (a_i - jb_i) f(\tau_E(n) + (n-i)T) e^{j\phi(n)} + \tilde{\eta}_e(n) \tag{3.14a}$$

$$y_0(n) = \sum_i (a_i - jb_i) f(\tau_E(n) + (n-i)T + T/2) e^{j\phi'(n)} + \tilde{\eta}_0(n). \tag{3.14b}$$

Since $|f_0 T| \ll 1$, we can make the approximation $\phi' = \phi$.

The two samples are then rotated by the estimated phase angle $\hat{\phi}(n)$ and filtered by the finite impulse response (FIR) filter $H(Z) = 1 + Z^{-1}$. The filtered samples are

$$\alpha_e(n) \approx (y_e(n) + y_0(n-1)) e^{j\phi_E(n)} = \sum_i (a_i - jb_i) \tilde{f}(\tau_E(n) + (n-i)T) e^{j\phi_E(n)} + \eta_e'(n) \tag{3.15a}$$

$$\alpha_0(n) \approx (y_0(n) + y_e(n)) e^{j\phi_E(n)} = \sum_i (a_i - jb_i) \tilde{f}(\tau_E(n) + (n-i)T + T/2) e^{j\phi_E(n)} + \eta_0'(n) \tag{3.15b}$$

where

$$\phi_E(n) = \phi(n) - \hat{\phi}(n) \text{ and } \eta_e'(n) = \tilde{\eta}_e(n) + \tilde{\eta}_0(n-1)$$

$$\tilde{f}(t) = f(t) + f(t - T/2) \qquad \eta_0'(n) = \tilde{\eta}_0(n) + \tilde{\eta}_e(n).$$

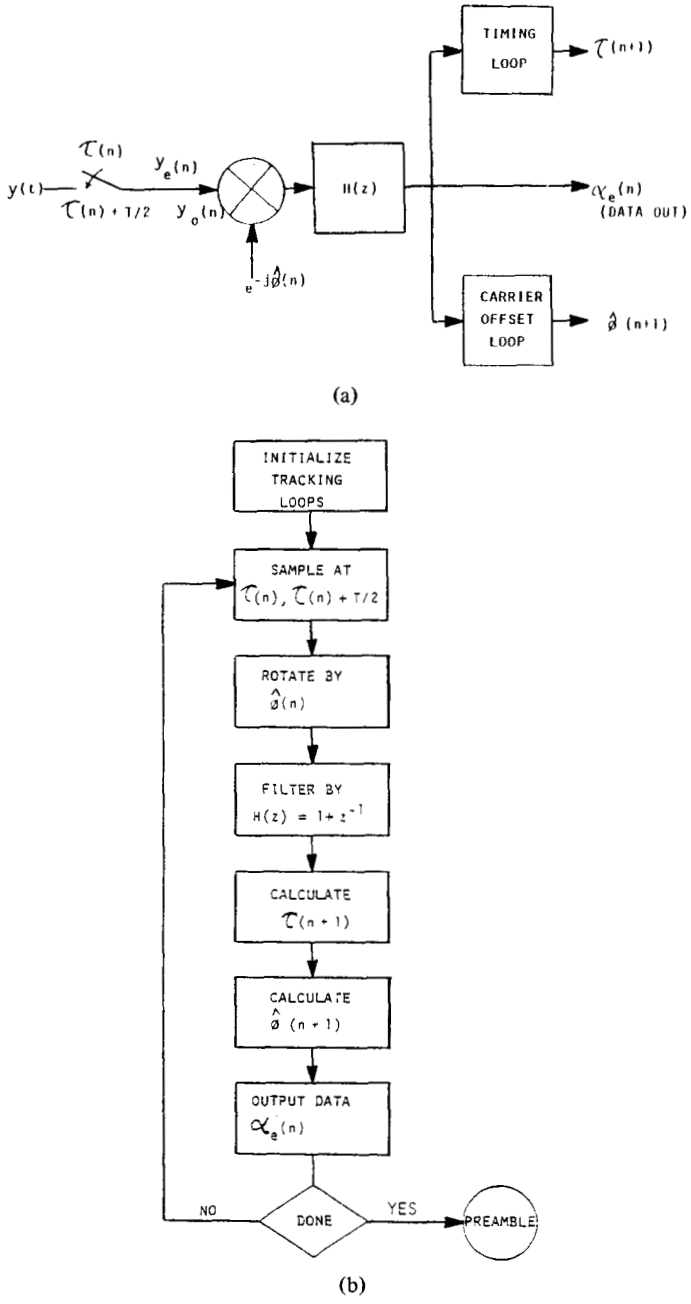

Figure 3.6. The Demodulation Stage of Processing. (a) Block Diagram. (b) Flowchart.

The FIR filter has a lowpass characteristic since the frequency response of this filter is proportional to $\cos(\pi fT)$. This filter reduces the effects of intersymbol interference (ISI) by shaping the spectrum of the signal such that the resulting pulse shape, $f(t)$, more closely approximates a Nyquist pulse ($\tilde{f}(t)|_{t=nT} = \delta(n)$).

The symbol timing function is performed on the real (I channel) portion of $\alpha_e(n)$, so that this algorithm can be used for both BPSK and QPSK packets (in the BPSK case, the imaginary signal is zero). The error signal for the symbol timing is based on the observation that (ignoring the effects of ISI and channel noise) when a data transition occurs in the real (in-phase) data, the real part of the odd samples, $\alpha_0(n)$ should

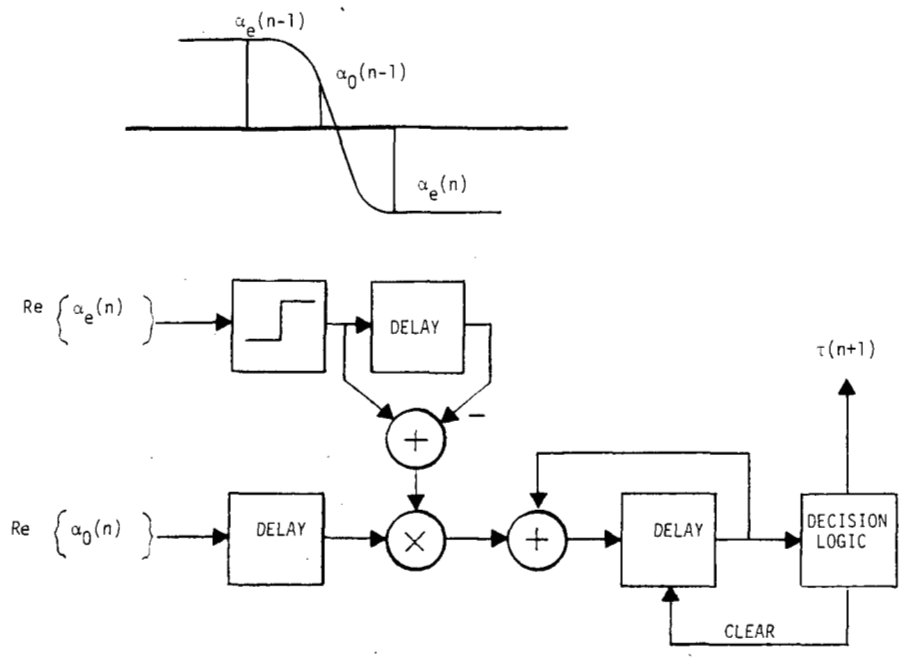

Figure 3.7. Symbol Phase Tracking.

be zero (see Figure 3.7). Therefore, we can derive the error signal as,**

$$\epsilon_T = \text{Re}\{\alpha_0(n-1)\} \cdot [\text{SGN}(\text{Re}\{\alpha_e(n-1)\}) - \text{SGN}(\text{Re}\{\alpha_e(n)\}]$$

$$\epsilon_T \approx [a_{n-1}\tilde{f}(\tau_E(n-1) + T/2) + a_n\tilde{f}(\tau_E(n) - T/2)] \cdot [\text{SGN}(a_{n-1}) - \text{SGN}(a_n)] + \eta$$

$$\approx \begin{cases} 0 & \text{if } a_n = a_{n-1} \\ 2|a_{n-1}|(\tilde{f}(\tau_E(n-1) + T/2) - \tilde{f}(\tau_E(n) - T/2)) + \eta & \\ \quad \text{if } a_n \neq a_{n-1}. \end{cases} \tag{3.16}$$

This assumes that the data decisions are correct*** (i.e., SGN (Re $\{\alpha_e(n)\}$) = SGN (a_n), etc.) where

$$\text{SGN}(x) = \begin{cases} 1 & x \geq 0 \\ -1 & x < 0. \end{cases}$$

This error signal is used to drive a first-order phase-locked loop (PLL). This loop is of the form,

$$\tau(n+1) = \tau(n) + K \cdot \epsilon_T \tag{3.17}$$

where K is a gain factor which is used to achieve a desired loop bandwidth. In the actual microprocessor, the sampling clock can be adjusted in discrete steps of $\Delta = T/128$ s only. The error signal is accumulated and, if the magnitude of the accumulator crosses a preset threshold, T_0, then the clock is incremented or decremented by Δ according to the sign of the accumulator. The accumulator is then set to zero (Figure 3.7), i.e.,

$$E_T(n) = E_T(n-1) + \epsilon_T(n) \tag{3.18}$$

$$\text{if } |E_T| < T_0 \Rightarrow \tau(n+1) = \tau(n)$$

$$\text{if } |E_T| \geq T_0 \Rightarrow \tau(n+1) = \tau(n) + \text{SGN}(E_T) \cdot \Delta; \quad E_T = 0.$$

In this algorithm the value of the threshold determines the loop bandwidth of the tracking loop. For QPSK packets, we can modify the error signal to include transitions in the imaginary (quadrature) channel by using equation (3.16) on this channel also.

The initialization of the symbol timing involves the adjustment of the sampling clock after the symbol phase is estimated in the first stage of processing. As discussed earlier, the symbol phase estimate is quantized to the four intervals centered at $\tau = 0$, $T/4$, $T/2$ and $3T/4$ which correspond to the maxima of the four γ_i's. The question that must be addressed is which of the four phases represents the desired timing for the second stage of processing. If, for the moment, we remove the FIR filter during the data demodulation stage (i.e., $H(Z) = 1$), then the phase corresponding to γ_0, i.e., $\tau = 0$, would be the desired phase since the even samples, $y_e(n)$, would be maximum, while the odd samples, $y_0(n)$, would be zero when a data transition occurred (see Figure 3.1). Thus, in this case, the sampling clock would be adjusted, based on the maximum γ_i, to the phase interval centered at $\tau = 0$. The FIR filter $H(Z) = 1 + Z^{-1}$ changes this picture slightly. Since the filter $H(Z) = 1 + Z^{-1}$ is a linear phase FIR filter with an even number of taps, it introduces a delay of $T/4$.[11] With this in mind, it becomes apparent that the desired phase interval is centered at $3T/4$ (the point where γ_2 is maximum). The sampling clock is adjusted accordingly.

** Re (·) is real part; Im (·) is imaginary part; η is the noise term.

*** The mean of ϵ_T resulting from incorrect decisions can also be computed in the same manner as the carrier phase tracking error mean is determined (see Appendix B).

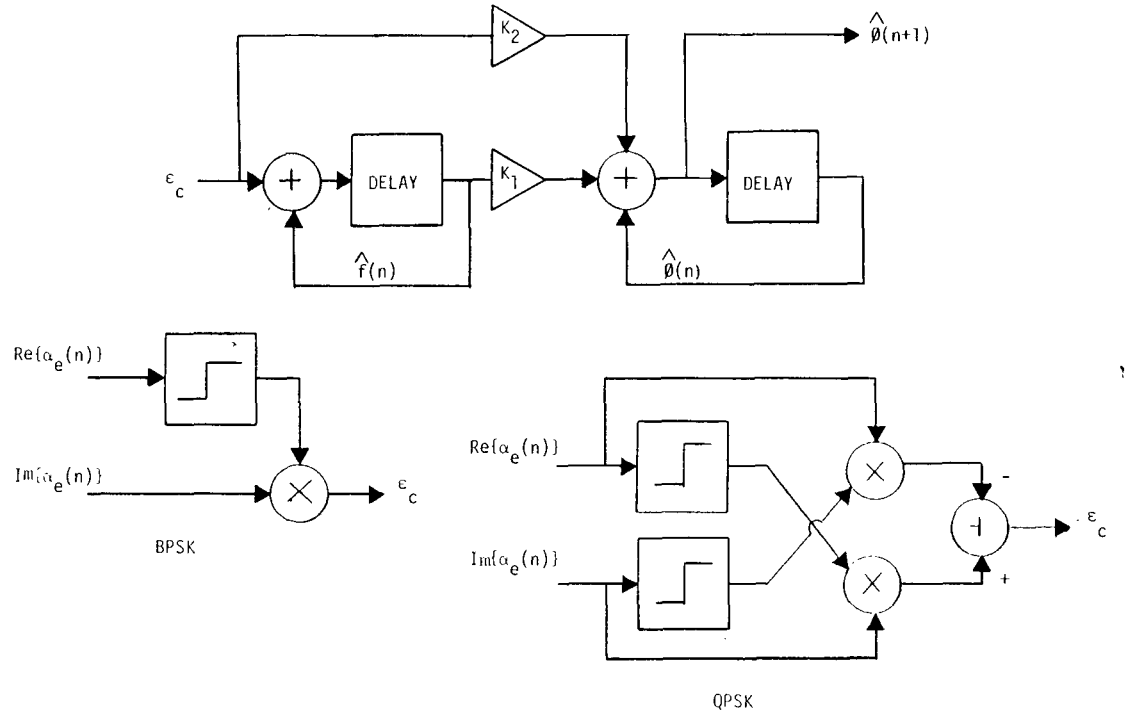

Figure 3.8. Carrier Offset Tracking.

The demodulation stage tracks the carrier offset frequency and phase with a numerical second-order phase-locked loop (see Figure 3.8). An error signal is derived, based on the data modulation (BPSK or QPSK) which is used to drive this tracking loop. Like the symbol timing loop, the tracking function is decision directed. For BPSK, the error signal is computed as,

$$\epsilon_c \equiv \text{Im}\{\alpha_e(n)\} \cdot \text{SGN}(\text{Re}\{\alpha_e(n)\}). \tag{3.19}$$

The expected value of this error signal in Gaussian noise is shown in Appendix B to be

$$\overline{\epsilon_c}(\phi_E) = |a_n| \sin(\phi_E) \cdot (1 - 2Q(\sqrt{\rho}\cos(\phi_E))) \tag{3.20}$$

where

$$\rho \equiv |a_n|^2 / E[\text{Re}\{\eta_e\}^2]$$

and

$$Q(x) = \frac{1}{\sqrt{2\pi}} \int_x^\infty e^{-y^2/2}\, dy.$$

A plot of the expected value of the error signal as a function of ϕ_E for $|a_n| = 1$ and various signal-to-noise ratios (ρ) is given in Figure 3.9. The fact that this function is periodic with period π is attributed to the two-way phase ambiguity that characterizes all BPSK systems.

For QPSK modulation, the error signal must make use of the knowledge that data are present in the imaginary (quadrature) channel, i.e.,

$$\epsilon_c \equiv \text{Im}\{\alpha_e(n)\} \cdot \text{SGN}(\text{Re}\{\alpha_e(n)\}) - \text{Re}\{\alpha_e(n)\} \cdot \text{SGN}(\text{Im}\{\alpha_e(n)\}). \tag{3.21}$$

The expected value of this error signal is shown in Appendix B to be,

$$\overline{\epsilon_c}(\phi_E) = \sqrt{2}\,|a_n| \cdot (g(\phi_E + \pi/4) + g(\phi_E - \pi/4)) \tag{3.22}$$

where $g(\phi) \equiv \sin(\phi) \cdot [1 - 2Q(\sqrt{2\rho}\cos(\phi))]$.

A plot of the expected value as a function of ϕ_E for various values of $\rho(|a_n| = 1/\sqrt{2})$ is also given in Figure 3.9. Note that, in this case, the value of ϕ_E is measured with respect to the line $e^{j\pi/4}$, i.e., the line where the real part is equal to the imaginary part. Again, the four-way phase ambiguity of QPSK modulation results in a periodic expected value (period = $\pi/2$).

The appropriate error signal is used to drive a second-order PLL which can be represented by the recursive relations (Figure 3.8),

$$\hat{\phi}(n+1) = \hat{\phi}(n) + k_1 \hat{f}(n) + k_2 \epsilon_c$$
$$\hat{f}(n+1) = \hat{f}(n) + \epsilon_c. \tag{3.23}$$

The resulting estimate $\hat{\phi}(n+1)$ is used to process the next data symbol. The constants K_1 and K_2 are adjusted to optimize the performance of this tracking function in the presence of noise.[2] The initialization of this carrier offset tracking loop is based upon scaled versions of the estimates obtained in the first stage of processing.

There is one other function which is performed by the processor during the demodulation stage. Both BPSK and QPSK modulation are characterized by a phase ambiguity which must be resolved by the processor. The technique which is used involves the transmission of a start-of-message (SOM) sequence after the preamble and before the data of the packet. The processor computes the correlation between the known sequence and the demodulated data. If the magnitude of the

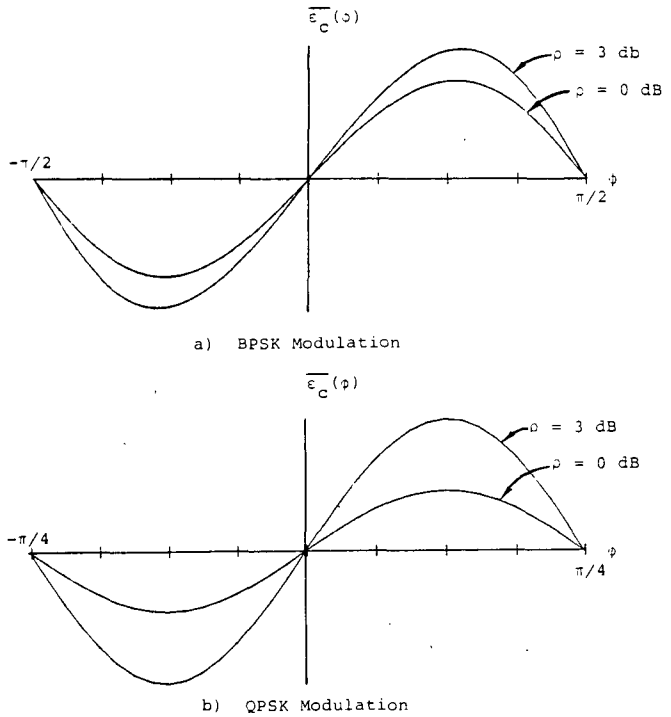

Figure 3.9. The Mean Value of the Error Signal in the Presence of Noise for BPSK and QPSK.

correlation crosses a set threshold, the start of data is declared and the phase ambiguity is resolved by the sign of the correlation. By the appropriate choice of SOM, this method has proven to be very effective in both frame synchronization and phase ambiguity resolution.

4.0 PERFORMANCE

The ability of the modem to successfully detect the preamble and efficiently demodulate the data portion of the packet, as measured by bit error rate, is directly related to the performance of the algorithms under actual operational conditions. The quantization of signals required by finite register length and processor computations, tend to degrade the performance of the algorithms. As a first step in evaluating performance, a computer simulation was developed on a general purpose computer†. This simulation included the effects of channel noise, intersymbol interference and finite register length. This FORTRAN program was used to gather statistics which were used to measure the influence of various parameters. The simulation helped to determine the level of quantization of the signal and to determine the implementation of processor functions, as well as to expose certain weak areas in the algorithms which could significantly degrade performance. For example, when the detection algorithm was simulated, it became apparent that a threshold could not be found which would give acceptable performance. If the threshold was low, then the algorithm tended to detect too early. As the threshold was raised, the random point in the preamble where detection is declared had an increasing variance, with the result that many packets were detected early and many detected late. The reason for this can be attributed to the fact that the energy of

† A DEC system 20.

TABLE 4.1
PROBABILITY OF MISSING A PACKET

E_s/N_0 (dB)	Probability of Not Detecting Packet	Probability of Missing Packet for Other Reasons	Total Probability of Missed Packet
1.0	8×10^{-3}	2.4×10^{-2}	3.2×10^{-2}
2.0	$< 10^{-4}$	4.9×10^{-3}	4.9×10^{-3}
3.0	$< 10^{-4}$	1.3×10^{-3}	1.3×10^{-3}
4.0	$< 10^{-4}$	$< 10^{-4}$	$< 10^{-4}$

the signal portion of the γ_i's climbs until the 64th received symbol, but remains constant for the remainder of the preamble (i.e., until the 96th symbol). A modification of the algorithm was made based on this "flattening" of the signal energy. The modified algorithm requires the maximum $\gamma_i(n)$ to cross a preset threshold for eight values of n in a row. This modification resulted in a significant reduction of the variance and gave a detection performance which was much improved.

The results of the simulations led to refinements of the algorithms and aided the development of the microprocessor which is used to implement these algorithms. The performance of the modem is measured in terms of (1) the probability of missing a packet and (2) the bit error rate of the data at the output of the demodulator. Missing packets can be attributed to two major causes. The first is the probability of not detecting the packet (or detecting it too late) due to the channel noise. Table 4.1 lists the measured probability of this occurrence for several values of signal-to-noise ratio. The other cause of missed packets is large errors in the estimates of symbol timing and/or carrier offset frequency and phase. When this occurs, the tracking loops are initialized incorrectly, which in turn means that they cannot "lock" onto the phase in a sufficiently short period of time. The reason for large errors in the preamble estimates may be attributed to a number of causes, but the most significant appears to be early detection of preamble. The probability of missing a packet for these reasons is also included in Table 4.1 as is the total probability of missing a packet.

The bit error rate performance is the other important modem performance measure in this packet format. Figure 4.1 shows bit error rate as a function of signal energy-to-noise density ratio. The lowest curve is the performance of ideal BPSK and QPSK over the infinite bandwidth, additive white Gaussian channel with matched filter detection.[2,3] The measured bit error rate performance of the actual microprogrammed processor is indicated by the circles. Notice that the performance is very close to optimum; at $E_s/N_0 = 1$ dB the loss due to both signal filtering and other losses (such as quantization) is less than .5 dB from ideal. The simulation results were very close to these points, which indicates the validity of both the models in this paper and those used in the simulation program.

5.0 IMPLEMENTATION AND APPLICATION

The microprocessor-based modem designed for a packet-switched network has been shown to operate with near opti-

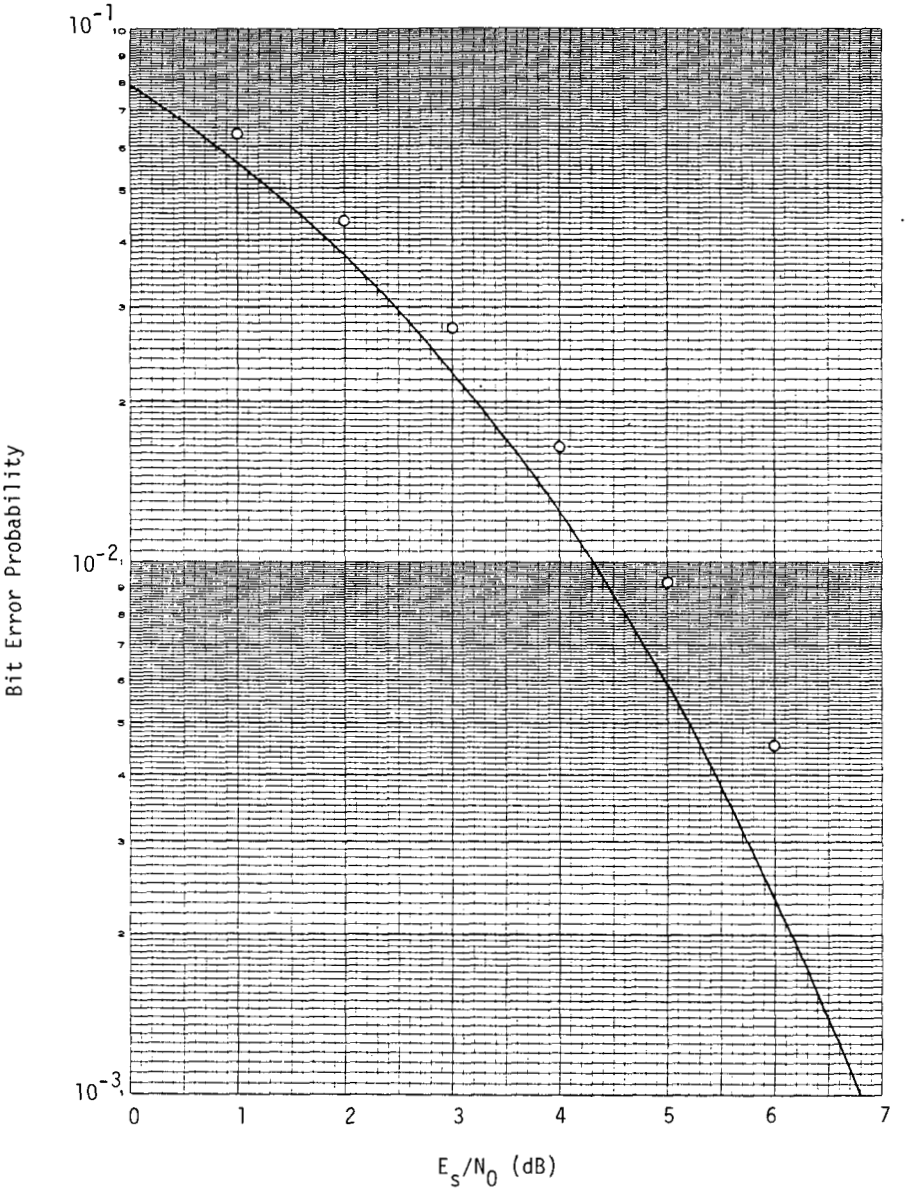

Figure 4.1. Bit Error Rate as a Function of Signal Noise Ratio.

mum performance over a band-limited, white Gaussian channel. The design of the demodulator involved two main areas of concentration: (1) the development of the demodulation algorithms which have been discussed in this paper, and (2) the architecture of the microprocessor. This single board machine is based on the AMD2901, a popular bipolar bit-slice processor, and the total number of IC's is 79 (see Figures 5.1 and 5.2). The implementation of the demodulation algorithm is in the form of a micro-instruction program which resides in read-only memories (ROM's). The design of the processor's architecture is such that the modem can be adapted to other types of modulation simply by changing software in the ROM's. For example, continuous or nonpacket modems can be implemented, as well as staggered QPSK or other digital modulation. It is estimated that a data rate of 100 kbits/s can be achieved with this processor.

The development of the modem was motivated by the needs of an experimental packet-switching network. The original network incorporates a few large stations which have large

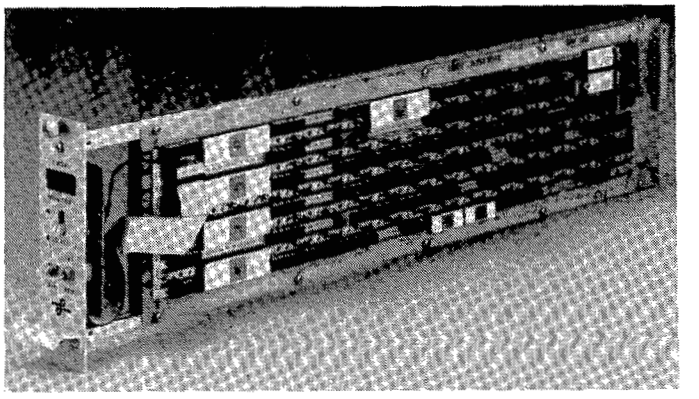

Figure 5.1. Digital Processor.

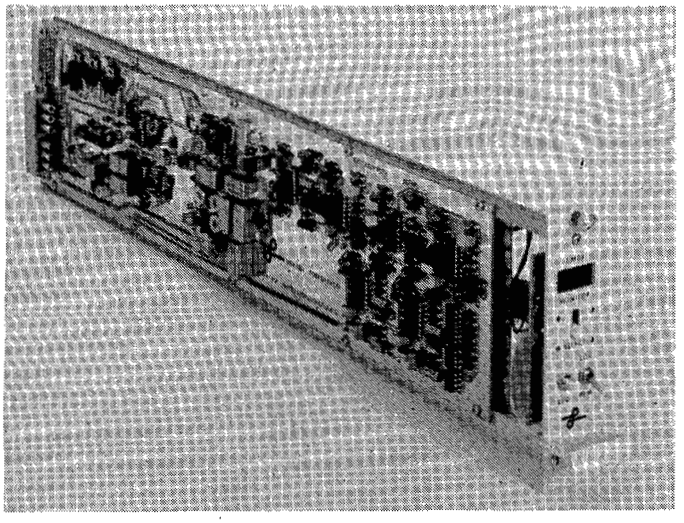

Figure 5.2. Analog Section.

antennas and low noise receivers. As expected, the operational signal-to-noise ratios are high. But the cost of constructing and maintaining a large number of these terminals is prohibitively expensive. To increase the size of the network, it becomes necessary to introduce less expensive small terminals into the system. To obtain acceptable performance of the network (in terms of throughput), it is necessary to operate with a bit error rate on the order of 10^{-4} or less. This is accomplished by the use of a demodulator which can operate with near optimum performance at the marginal signal-to-noise ratios which characterize the small station. In addition, use of convolutional encoding-Viterbi decoding is necessary to reduce the required signal-to-noise ratios even further. An important aspect of efficient decoding is the ability to use soft quantized estimates of the encoded symbols in the decoding process. The availability of these soft decisions at the output of the demodulator is an important feature of the modem. Of course, the data rate of the channel is reduced by a factor of two (rate 1/2 code), but without the availability of this efficient demodulation/decoding combination, the incorporation of the small stations in the network would not have been feasible.

The flexibility afforded by microprocessor implementation has been fully demonstrated in this application. New modes and additional features, such as digital monitoring of various modem parameters and built-in testing are continuing to be added by field installation of reprogrammed ROM's.

APPENDIX A

COMPLEX SIGNAL MODEL

The complex model of Figure 2.1 is derived from a model which consists of entirely real signals. The quadrature signal communication modem can be described with the aid of Figure A.1. Two data signals, $x_1(t)$ and $x_2(t)$, are to be transmitted over the in-phase and quadrature phase channels, respectively. These signals represent antipodal data modulated by a rectangular pulse of duration T,

$$x_1(t) = \sum_i a_i p(t - iT)$$

$$x_2(t) = \sum_i b_i p(t - iT) \tag{A.1a}$$

$$p(t) = \begin{cases} 1 & -T/2 \leqslant t < T/2 \\ 0 & \text{otherwise.} \end{cases} \tag{A.1b}$$

The a_i's and b_i's represent the data and are equal to $\pm 1/\sqrt{2}$ (thus $a_i^2 + b^2 = 1$). For BPSK modulation, we may take $a_i = \pm 1$ and $b_i = 0$ or, equivalently, $a_i = b_i = \pm 1/\sqrt{2}$ (which is used in Section 2.0). These two signals are then used to modulate sine and cosine carriers of frequency f_1 respectively, and then summed. The result is passed through a bandpass filter $H_1(f)$ centered at f_1. It is then transmitted over an additive white Gaussian noise (AWGN) channel with (two-sided) spectral density $N_0/2$. The received signal is mixed to near baseband using two quadrature sinewaves of frequency f_2 and phase ϕ. It is assumed that the difference between f_1 and f_2 is small compared to the data rate, $1/T$, i.e.,

$$|f_0 T| \ll 1 \text{ where } f_0 = f_1 - f_2.$$

The two resulting signals are passed through a lowpass filter $H_2(f)$, which removes the sum frequency terms $(f_1 + f_2)$. The resulting waveforms are:

$$\begin{aligned} y_1(t) = \sum_i a_i \iint & p(t - iT - \tau - \sigma) h_1'(\sigma) h_2(\tau) \\ & \cdot \cos(2\pi f_0(t - \tau) + \phi)\, d\sigma d\tau \\ & + b_i \iint p(t - iT - \tau - \sigma) h_1'(\sigma) h_2(\tau) \\ & \cdot \sin(2\pi f_0(t - \tau) + \phi)\, d\sigma d\tau + \sqrt{2} \int \eta(t - \tau) h_2(\tau) \\ & \cdot \cos(2\pi f_2(t - \tau) + \phi)\, d\tau \end{aligned} \tag{A.2a}$$

$$\begin{aligned} y_2(t) = \sum_i a_i \iint & p(t - iT - \tau - \sigma) h_1'(\sigma) h_2(\tau) \\ & \cdot \sin(2\pi f_0(t - \tau) + \phi)\, d\sigma d\tau \\ & - b_i \iint p(t - iT - \tau - \sigma) h_1'(\sigma) h_2(\tau) \\ & \cdot \cos(2\pi f_0(t - \tau) + \phi)\, d\sigma d\tau + \sqrt{2} \int \eta(t - \tau) h_2(\tau) \\ & \cdot \sin(2\pi f_2(t - \tau) + \phi)\, d\tau. \end{aligned} \tag{A.2b}$$

Note that $h_1'(t)$ is the impulse response of the filter which is the complex envelope of $H_1(f)$. Since it is assumed that $H_1(f)$ was centered at f_1, the impulse response $h_1'(t)$ is real.[4] It is convenient to define the complex signal $y(t)$,

$$\begin{aligned} y(t) &\equiv y_1(t) + j y_2(t) \\ &= \sum_i (a_i - j b_i) f(t - iT) e^{j[2\pi f_0 t + \phi]} + \tilde{\eta}(t) \end{aligned} \tag{A.3}$$

where

$$f(t) = \iint p(t - \sigma - \tau) h_1'(\sigma) h_2(\tau) e^{-j2\pi f_0 \tau}\, d\sigma d\tau$$

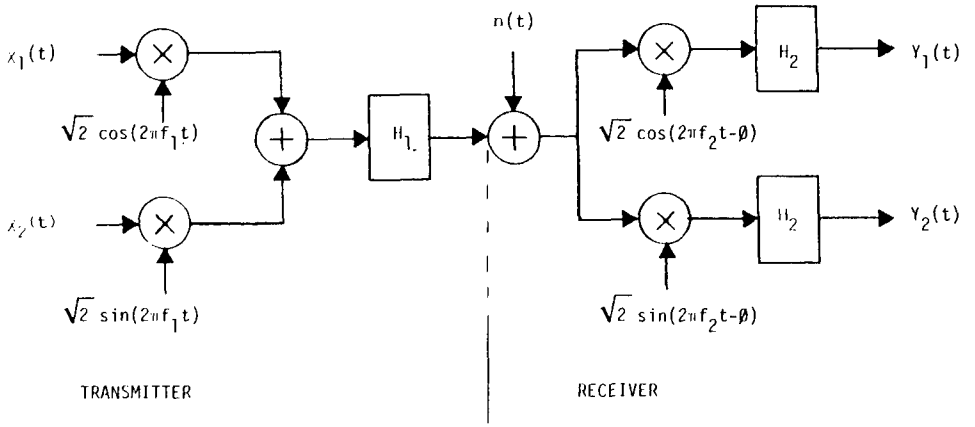

Fig. A1. The QPSK/BPSK Model (Real Signals).

and

$$\tilde{\eta}(t) \equiv \tilde{\eta}_0(t) + j\tilde{\eta}_2(t) = \int \eta(t-\tau) e^{j[2\pi f_2(t-\tau)+\phi]} h_2(\tau)\, d\tau.$$

This complex model is used throughout this paper where the transmitted signal is

$$x(t) \equiv x_1(t) - jx_2(t)$$

and the channel introduces

$$\eta(t) \equiv \eta_1(t) + j\eta_2(t)$$

which is complex white Gaussian noise.

APPENDIX B
THE EXPECTED VALUES OF THE CARRIER OFFSET PHASE-ERROR SIGNAL

The carrier offset phase error ϵ_c for the BPSK case is

$$\epsilon_c \equiv y \cdot \mathrm{SGN}(x),$$

where

$$\alpha_e(n) = a_n e^{j\phi_E} + \eta_e(n) \equiv x + jy$$
$$x = a_n \cos\phi_E + \mathrm{Re}\{\eta_e(n)\}$$
$$\bar{x} \equiv a_n \cos\phi_E$$
$$y = a_n \sin\phi_E + \mathrm{Im}\{\eta_e(n)\}$$
$$\bar{y} \equiv a_n \sin\phi_E.$$

Using the fact that the noise is zero-mean Gaussian and that the noise in the I-channel is uncorrelated with the noise in the Q-channel, we can find the expected value of ϵ_c as a function of phase error ϕ_E,

$$\overline{\epsilon_c}(\phi_E) = \bar{y} \cdot E[\mathrm{SGN}(x)]$$
$$= \bar{y} \cdot [1 - 2P(x \leqslant 0)]$$
$$= a_n \sin(\phi_E) \cdot \left[1 - 2Q\left(\frac{a_n}{\sigma}\cos(\phi_E)\right)\right]$$
$$= |a_n| \sin(\phi_E) \cdot [1 - 2Q(\sqrt{\rho}\cos(\phi_E))]$$

where $\rho \equiv a_n{}^2/\sigma^2$, $\sigma^2 \equiv E[\mathrm{Re}\{\alpha_e(n)\}^2]$

$$Q(x) = \frac{1}{\sqrt{2\pi}}\int_x^\infty e^{-y^2/2}\, dy.$$

The last step uses the fact that the function $[1 - 2Q(x)]$ is an odd function in x.

The expected value for the QPSK case is a more tedious calculation, but uses the same basic concepts. Here,

$$\epsilon_c = y \cdot \mathrm{SGN}(x) - x \cdot \mathrm{SGN}(y)$$

where

$$\alpha_e(n) = (a_n - jb_n)e^{j\phi_E} + \eta_e(n) \equiv x + jy$$
$$x = a_n \cos(\phi_E) + b_n \sin(\phi_E) + \mathrm{Re}\{\eta_e(n)\}$$
$$\bar{x} \equiv a_n \cos(\phi_E) + b_n \sin(\phi_E)$$
$$= \sqrt{2}\,|a_n|\,\mathrm{SGN}(a_n)\cos(\phi_E - \mathrm{SGN}(a_n)\,\mathrm{SGN}(b_n) \cdot \pi/4)$$
$$= \sqrt{2}\,|a_n|\,\mathrm{SGN}(b_n)\sin(\phi_E + \mathrm{SGN}(a_n)\,\mathrm{SGN}(b_n) \cdot \pi/4)$$
$$y = a_n \sin(\phi_E) - b_n \cos(\phi_E) + \mathrm{Im}\{\eta_e(n)\}$$
$$\bar{y} \equiv a_n \sin(\phi_E) - b_n \cos(\phi_E)$$
$$= -\sqrt{2}\,|a_n|\,\mathrm{SGN}(b_n)\cos(\phi_E + \mathrm{SGN}(a_n)\,\mathrm{SGN}(b_n) \cdot \pi/4)$$
$$= \sqrt{2}\,|a_n|\,\mathrm{SGN}(a_n)\sin(\phi_E - \mathrm{SGN}(a_n)\,\mathrm{SGN}(b_n) \cdot \pi/4).$$

We use the fact that $|a_n| = |b_n|$ in computing the many forms of $\bar{x}$ and $\bar{y}$. We can now take the expected value,

$$\overline{\epsilon_c}(\phi_E) = \bar{y} \cdot E[\mathrm{SGN}(x)] - \bar{x} \cdot E[\mathrm{SGN}(y)]$$
$$= \sqrt{2}\,|a_n|\sin(\phi_E - \mathrm{SGN}(a_n)\,\mathrm{SGN}(b_n) \cdot \pi/4)$$
$$\cdot \left[1 - 2Q\left(\sqrt{2}\,\frac{|a_n|}{\sigma}\cos(\phi_E - \mathrm{SGN}(a_n)\,\mathrm{SGN}(b_n) \cdot \pi/4)\right)\right]$$
$$+ \sqrt{2}\,|a_n|\sin(\phi_E + \mathrm{SGN}(a_n)\,\mathrm{SGN}(b_n) \cdot \pi/4)$$
$$\cdot \left[1 - 2Q\left(\sqrt{2}\,\frac{|a_n|}{\sigma}\cos(\phi_E - \mathrm{SGN}(a_n)\,\mathrm{SGN}(b_n) \cdot \pi/4)\right)\right]$$
$$\overline{\epsilon_c}(\phi_E) = \sqrt{2}\,|a_n|\,[g(\phi_E + \pi/4) + g(\phi_E - \pi/4))$$

where

$$g(\phi) = \sin(\phi) \cdot [1 - 2Q(\sqrt{2\rho}\cos(\phi))].$$

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Jerrold A. Heller (M'68) received the B.E.E. degree Magna Cum Laude from Syracuse University in 1963, and the M.S. and Ph.D. degrees in Electrical Engineering in 1964 and 1967, respectively, from the Massachusetts Institute of Technology.

During this period he held summer employment at Bell Telephone Laboratories and IBM Research Laboratory, Yorktown Heights, New York. From 1967 until 1969, Dr. Heller was with the Communication Systems Research Section of the Jet Propulsion Laboratory where his work involved analysis, simulation, and software implementation of coded systems for space communication channels. Since joining LINKABIT Corporation in September 1969 as Director of Engineering, Dr. Heller has led studies and hardware and software implementation of coded communication systems for satellite, HF, and telephone line channels. Among the projects he has initiated and led are the discovery and implementation of a new type of syndrome feed-back decoder for convolutional codes, several novel techniques for Viterbi decoder implementation, the implementation of a soft decision sequential decoder operating at 3 megacomputations/s, and development of a real time digital television compression system which allows digital transmission of NTSC video at 8 Mbits/s. Recently, Dr. Heller led a development effort for a microprocessor-implemented 32- and 64-Kbit/s BPSK/QPSK packet satellite communication modem, employing a bipolar microprocessor with an architecture specifically designed for signal processing functions under this project.

In 1974, Dr. Heller was appointed Vice President, Engineering by LINKABIT's Board of Directors.

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Andrew J. Viterbi (S'54-M'58-SM'63-F'73) received the B.S. and M.S. degrees in Electrical Engineering in 1957 from the Massachusetts Institute of Technology. In 1962 he received the Ph.D. degree in Electrical Engineering from the University of Southern California.

From 1957 to 1963, Dr. Viterbi was with the Communication Research Section of the Jet Propulsion Laboratory where he rose to the position of Research Group Supervisor. In 1963 he joined the faculty of the University of California, Los Angeles, where he rose to become Professor of Engineering and Applied Science in 1969. In 1973 he took an industrial leave of absence to devote his full-time efforts as Vice President of LINKABIT Corporation, which he participated in founding in 1968. In 1975 he resigned from UCLA and accepted the title of Adjunct Professor of Applied Physics and Information Science at the University of California, San Diego. In 1974 he was elected to the newly created position of Executive Vice President of LINKABIT Corporation.

Dr. Viterbi has been active in professional groups of the IEEE in various capacities on both the local and national levels. From 1964 through 1970, and again since 1976, he has been a member of the Ad Com/Board of Governors of the Information Theory Group and served as Group Chairman in 1970. Since 1967 he has been a member of the Editorial Board of the journal *Information and Control;* from 1969 to 1977, a member of the Editorial Board of the *IEEE Proceedings;* from 1971 to 1975, an Associate Editor of the *IEEE Transactions on Information Theory.* He has served as a member of advisory committees and as a consultant for the U.S. Air Force, NASA, and the U.S. Army, including the Army Scientific Advisory Panel.

Dr. Viterbi is the co-author of a book on digital communication and author of the first text on coherent communication. He has received various awards for his publications, including the 1968 IEEE Information Theory Group Outstanding Paper Award and the 1975 Christopher Columbus International Communications Award.